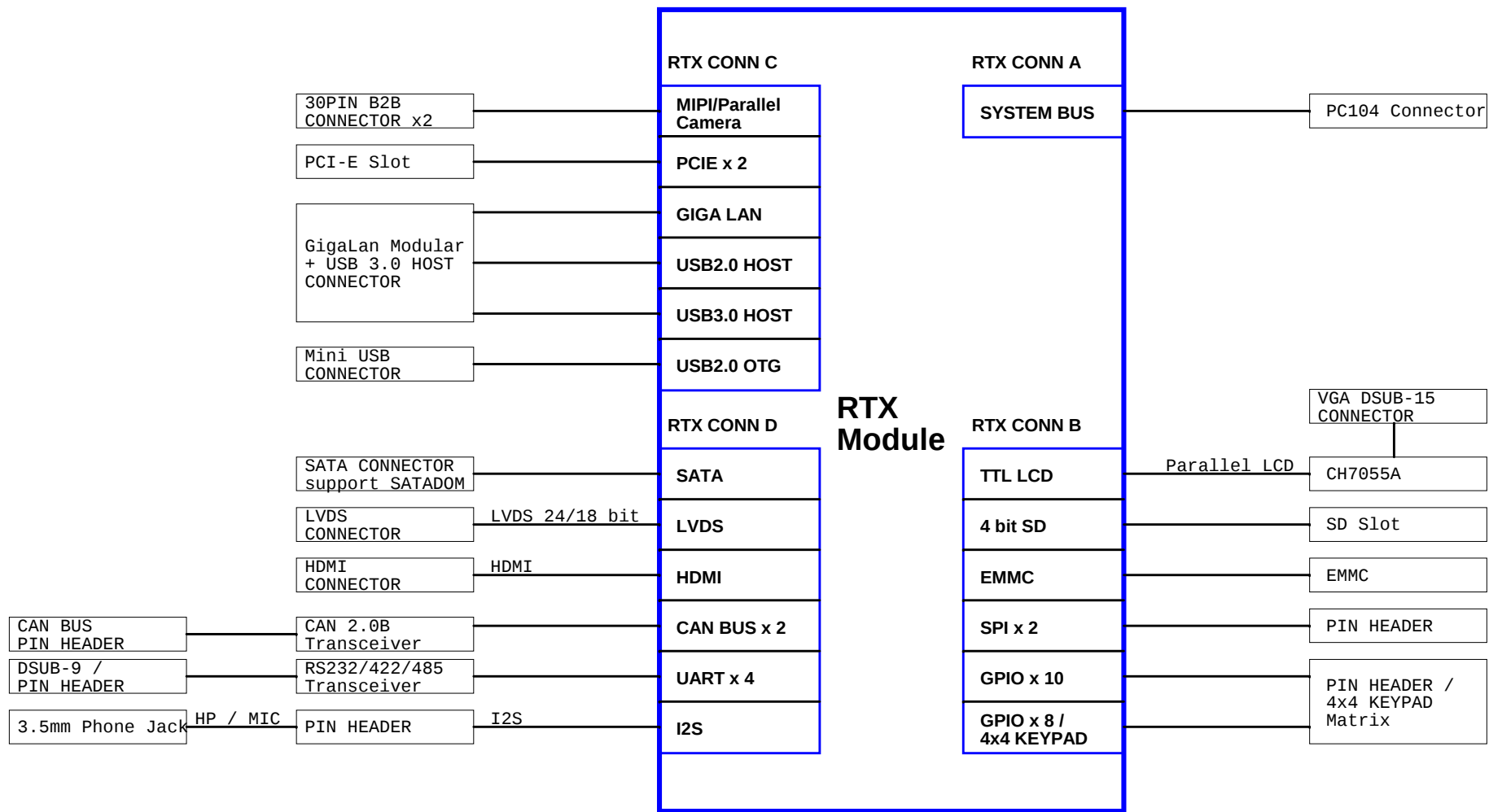


Model Name: ROM-DB3900

01	COVER PAGE
02	BLOCK DIAGRAM
03	POWER BLOCK DIAGRAM
04	POWER ENABLE SEQUENCE
05	DC IN
06	RTX Module Power
07	+V12
08	+V5
09	+V3
10	TTL to VGA
11	LVDS
12	HDMI
13	USB OTG
14	GigaLAN & USB HOST
15	PCI-E
16	SATA, SDIO, EMMC, I2C EEPROM
17	CAN BUS
18	UART0/1
19	UART2/3
20	I2S
21	Camera
22	SPI, LED, GPIO, Keypad
23	BUTTON, BOOTSEL, WDT, FAN
24	SYSTEM BUS
25	RTX B2B CONNECTOR
26	HISTORY



+ADP_MAIN

+V3A

+VDD_CORE

+V3

+V5

+V12

+ADP_MAIN to +V3A > 0ms

+ADP_MAIN to +VDD_CORE > 0ms

+VDD_CORE to +V3 > 0ms

+V3 to +V5 > 0ms

+V5 to +V12 > 0ms

ADVANTECH

Title POWER ENABLE SEQUENCE

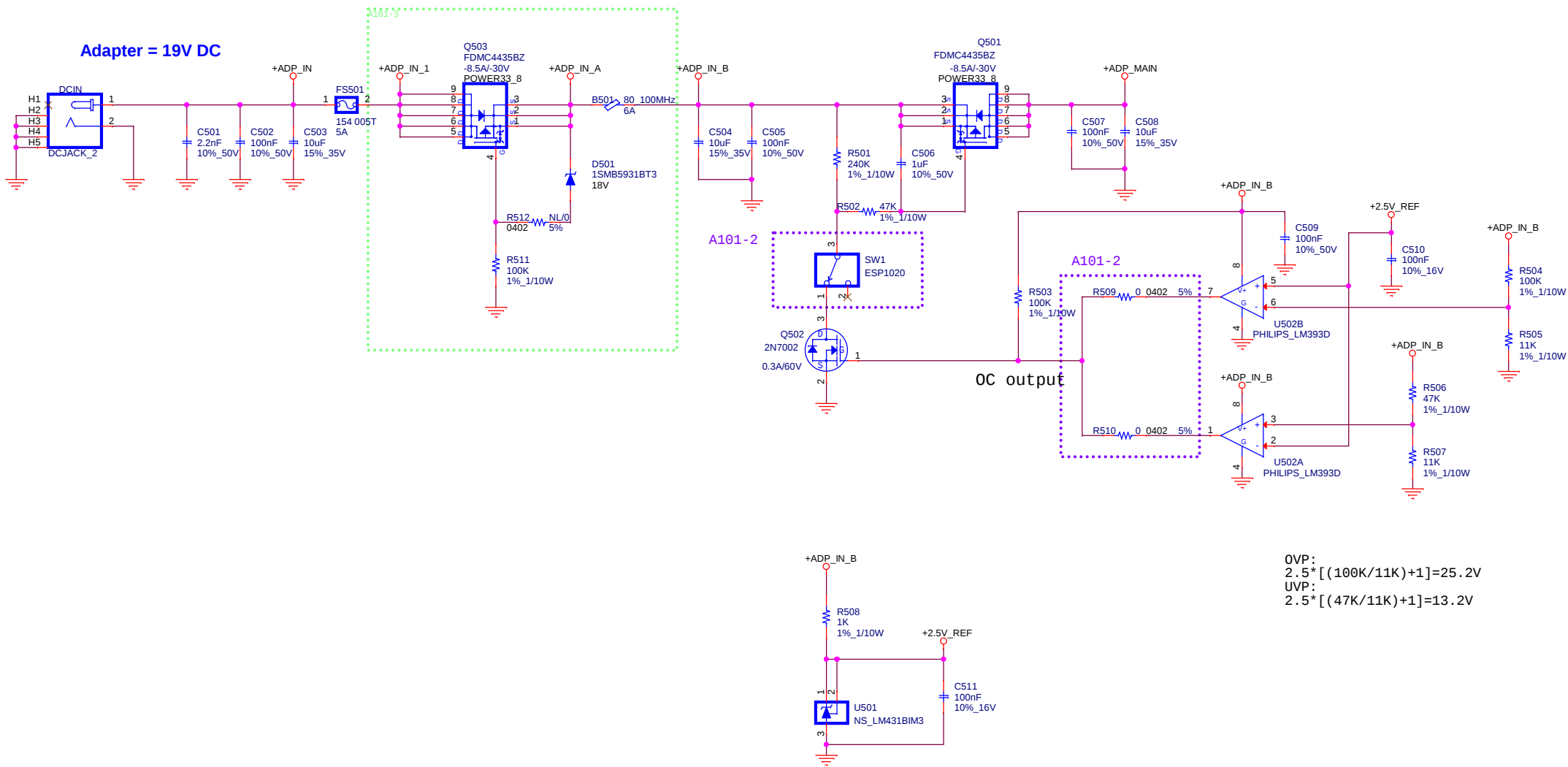
Size Document Number ROM-DB3900

Date: Friday, December 04, 2015

Rev A101-3

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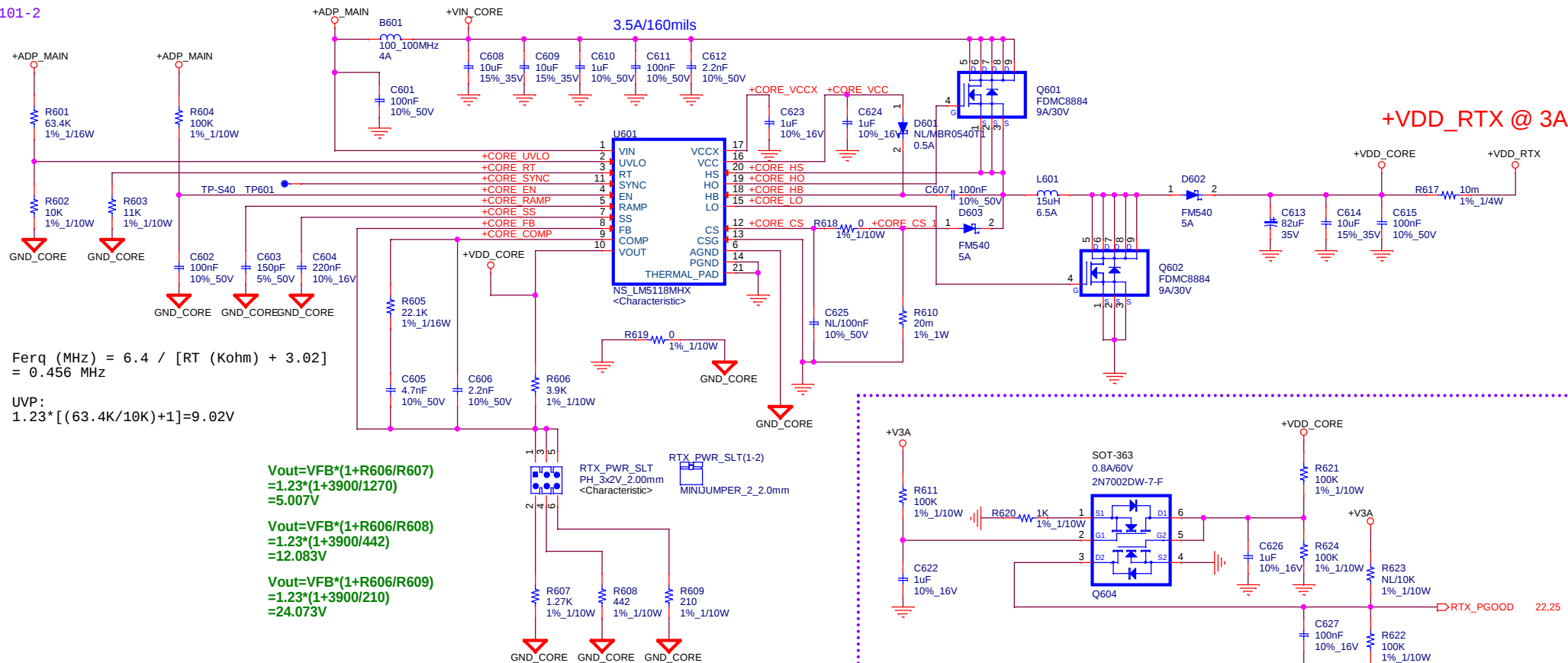
Adapter = 19V DC



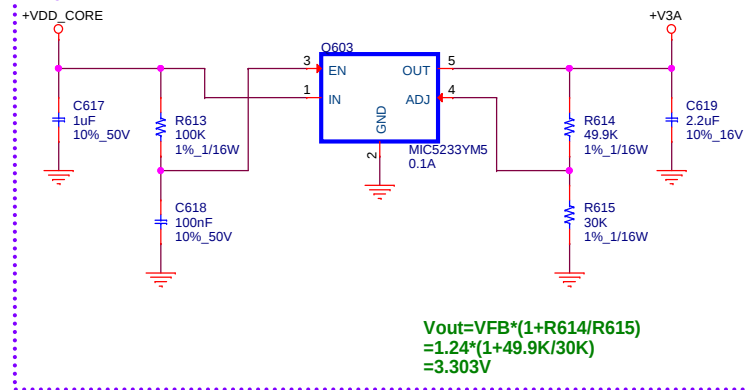
OVP:
 $2.5 * [(100K/11K)+1] = 25.2V$
 UVP:
 $2.5 * [(47K/11K)+1] = 13.2V$

ADVANTECH			
Title		DC IN	
Size	Document Number	ROM-DB3900	Rev
Date:		Friday, December 04, 2015	Sheet 5 of 26

A101-2



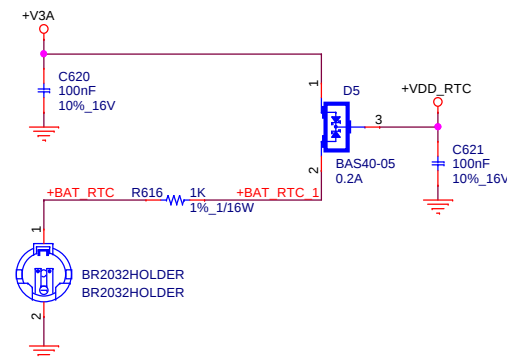
A101-2



BAT

Li Battery 3V BR2032

BR2032 3V_195mAH



ADVANTECH

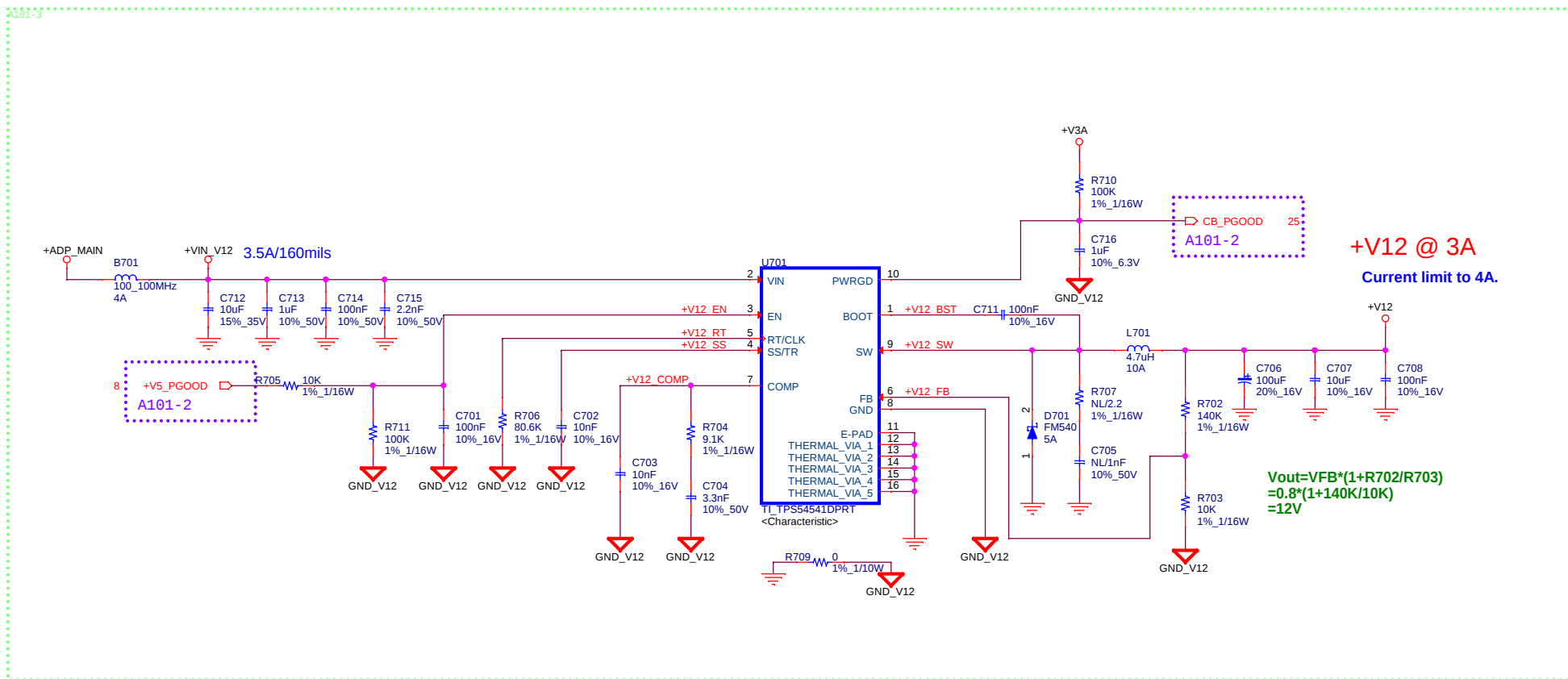
Title RTX Module Power

Size Document Number ROM-DB3900

Date: Friday, December 04, 2015

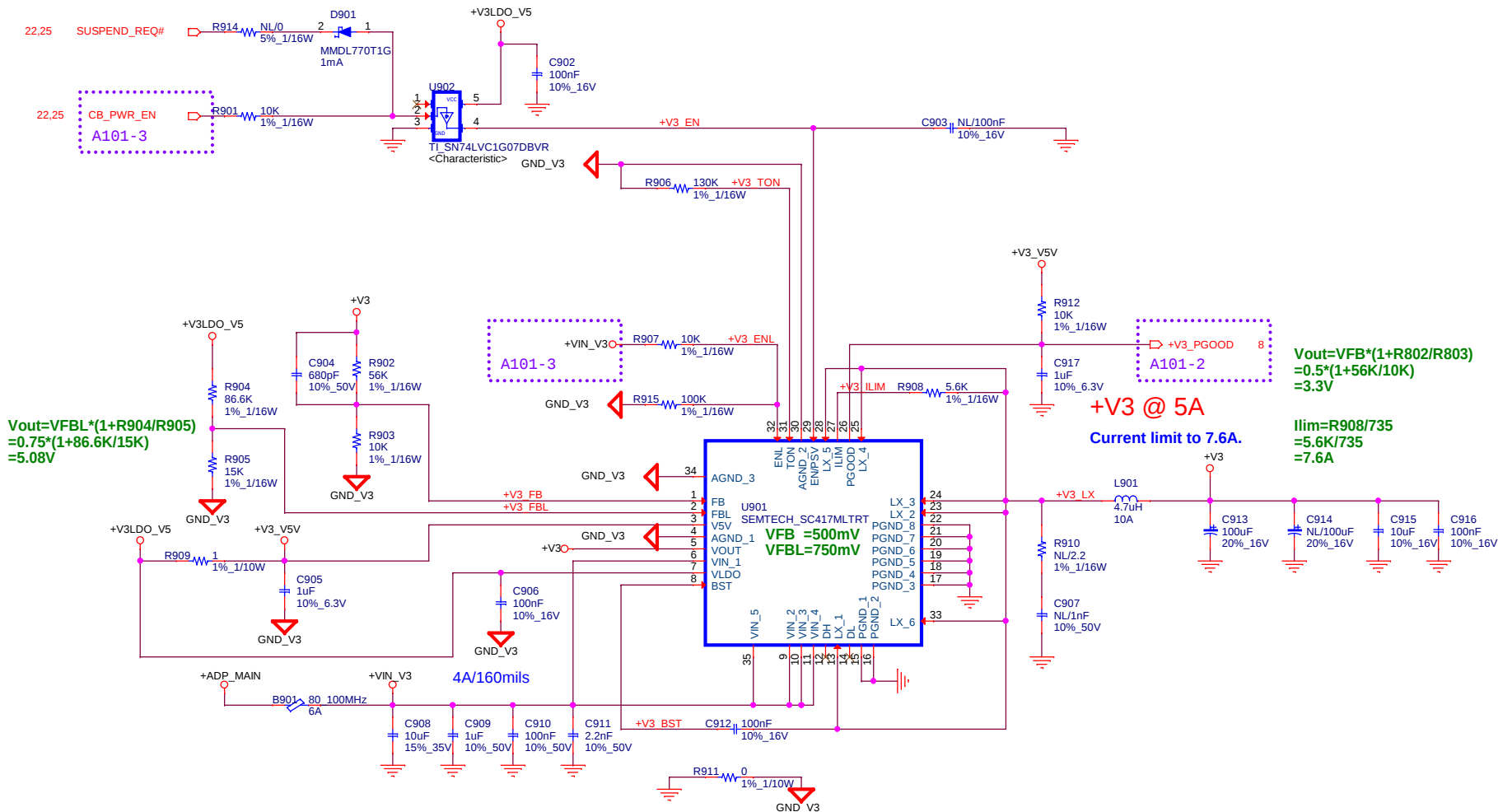
Sheet 6 of 26

Rev A101-3

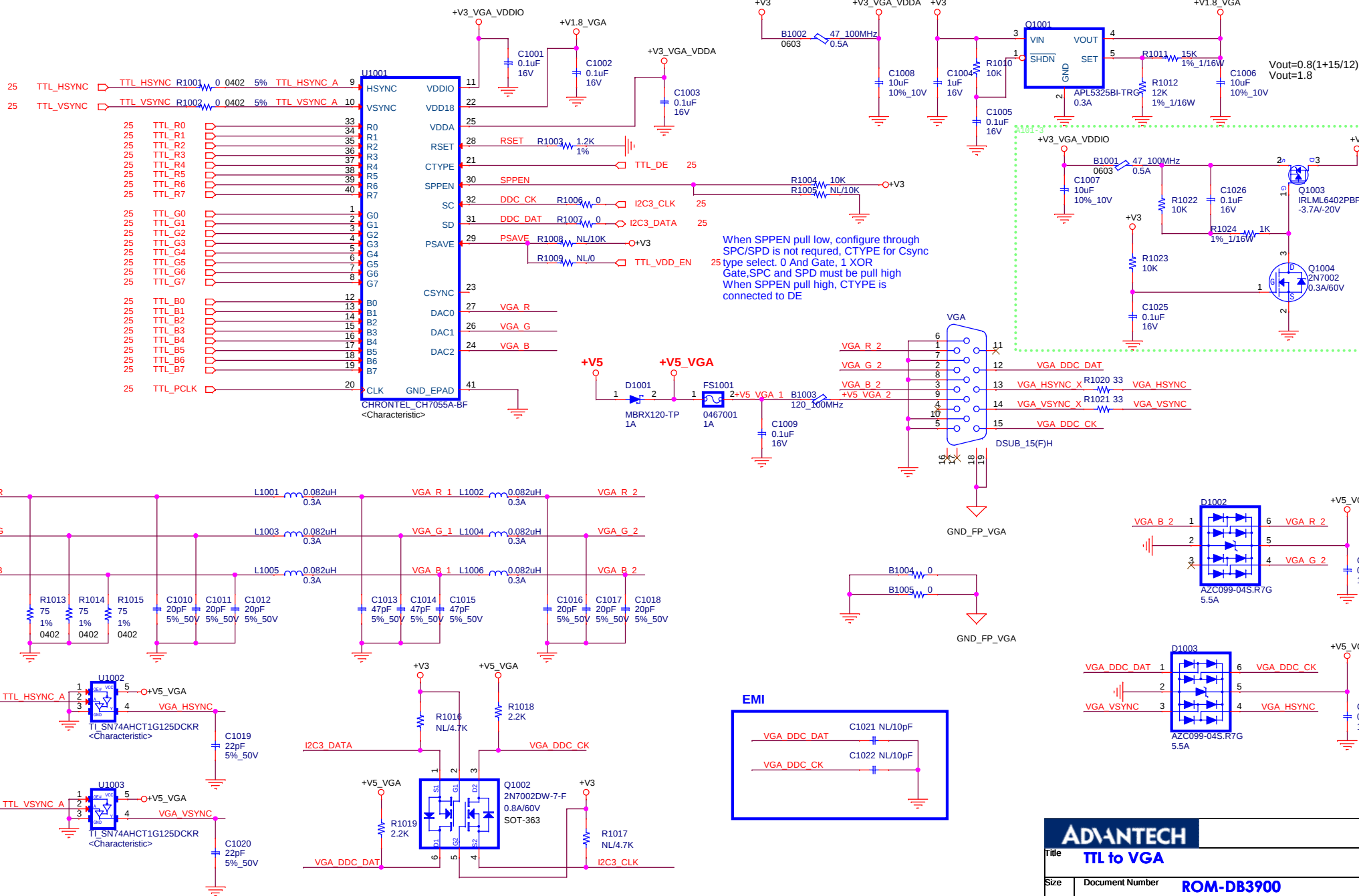


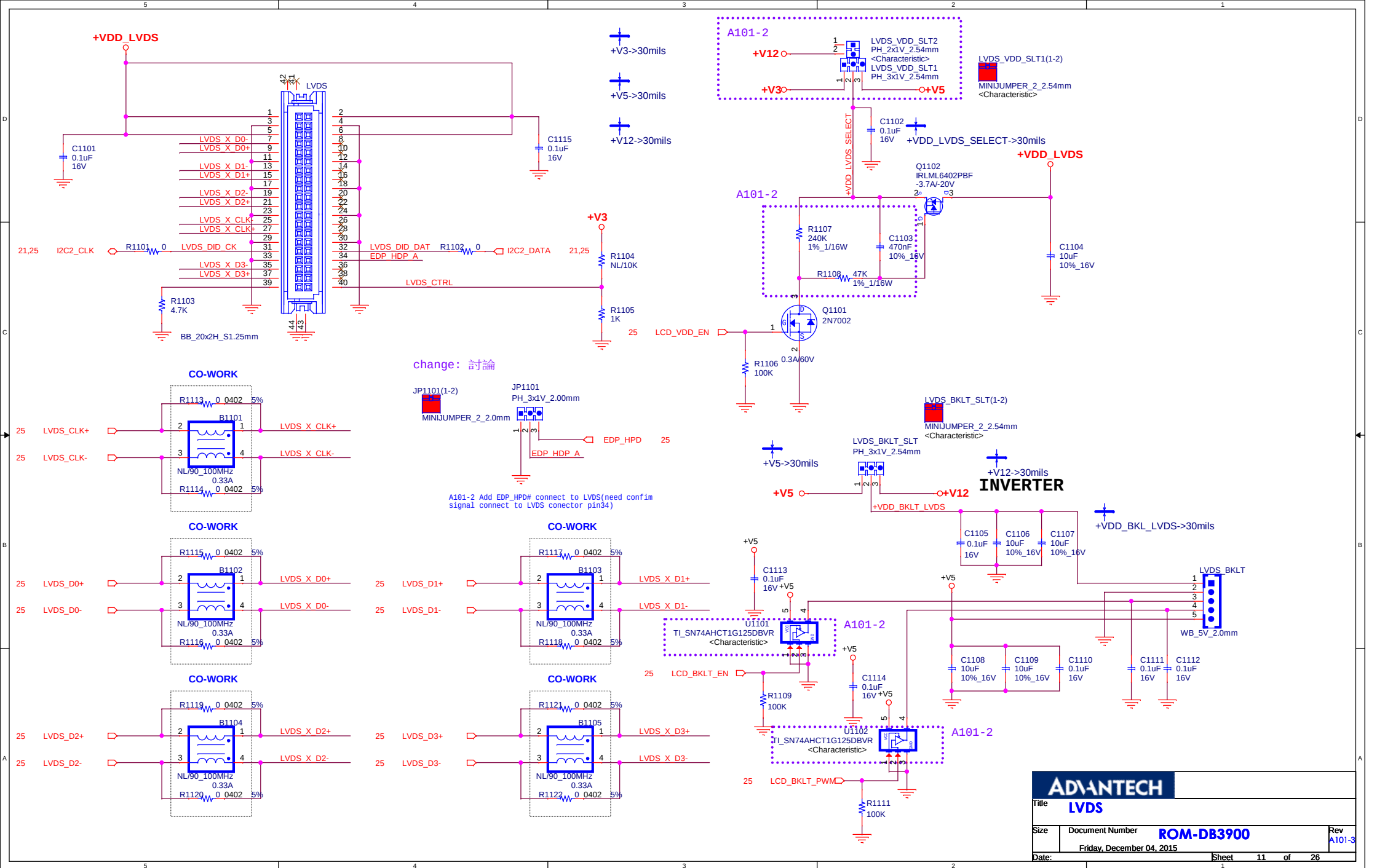
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Title		+V12	
Size	Document Number	ROM-DB3900	
Date:	Friday, December 04, 2015	Sheet	7 of 26
		Rev	A101-3

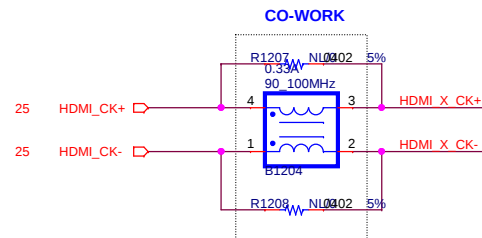
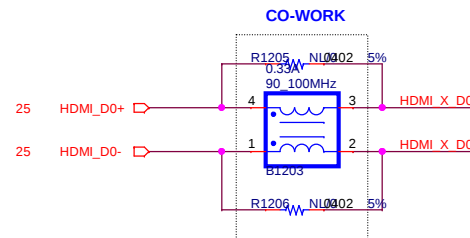
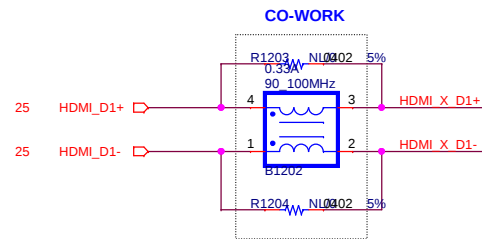
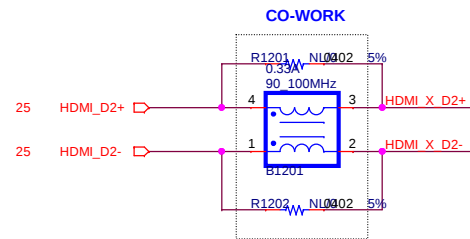
+V3



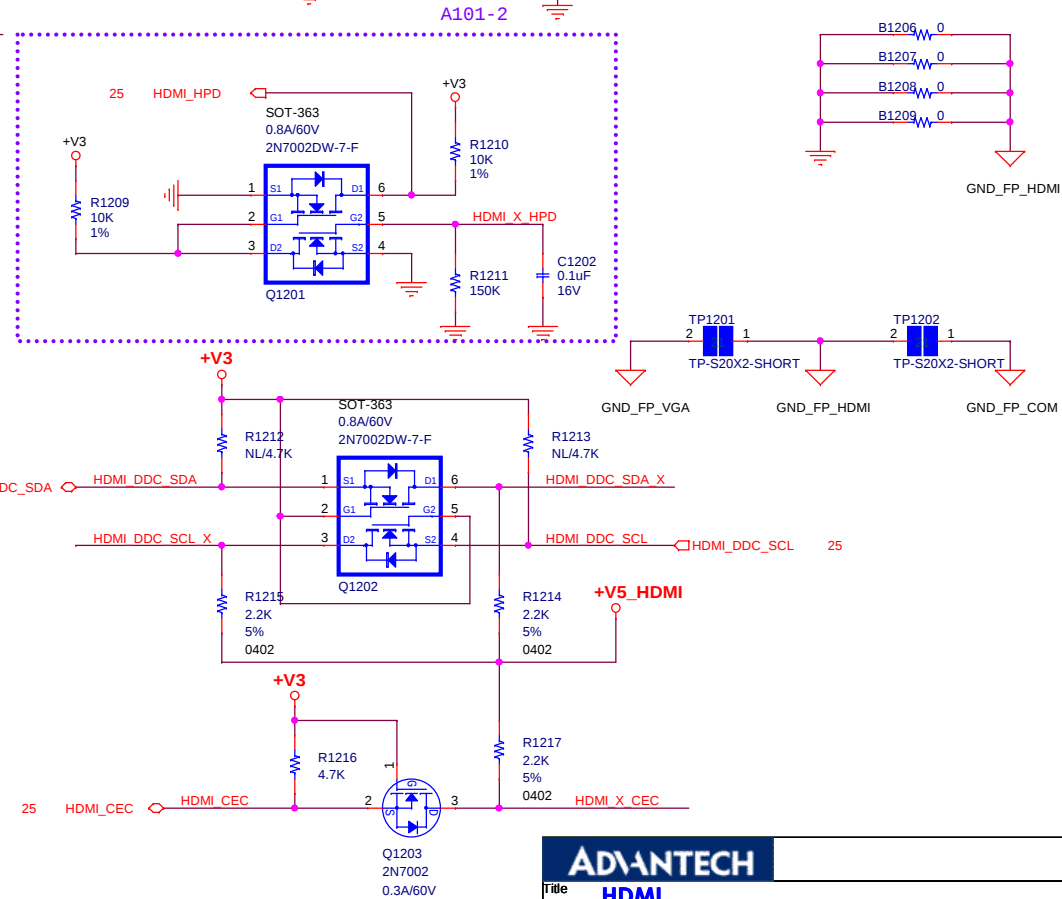
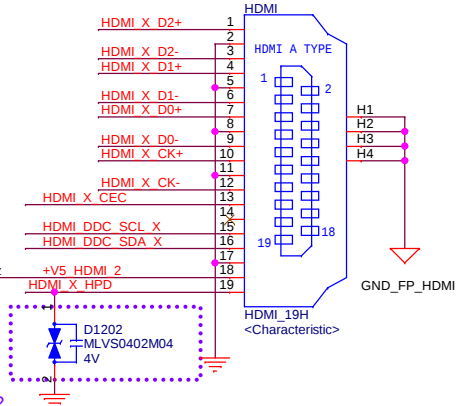
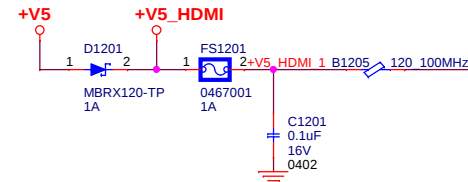
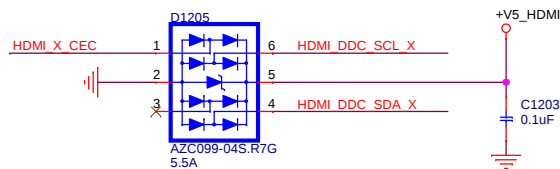
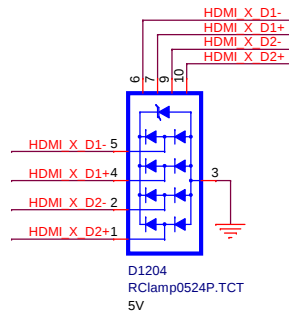
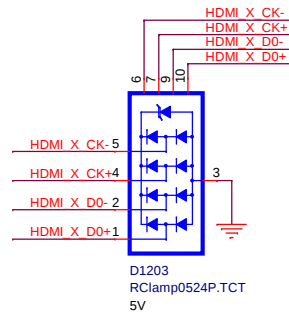
ADVANTECH			
Title +V3			
Size	Document Number	ROM-DB3900	
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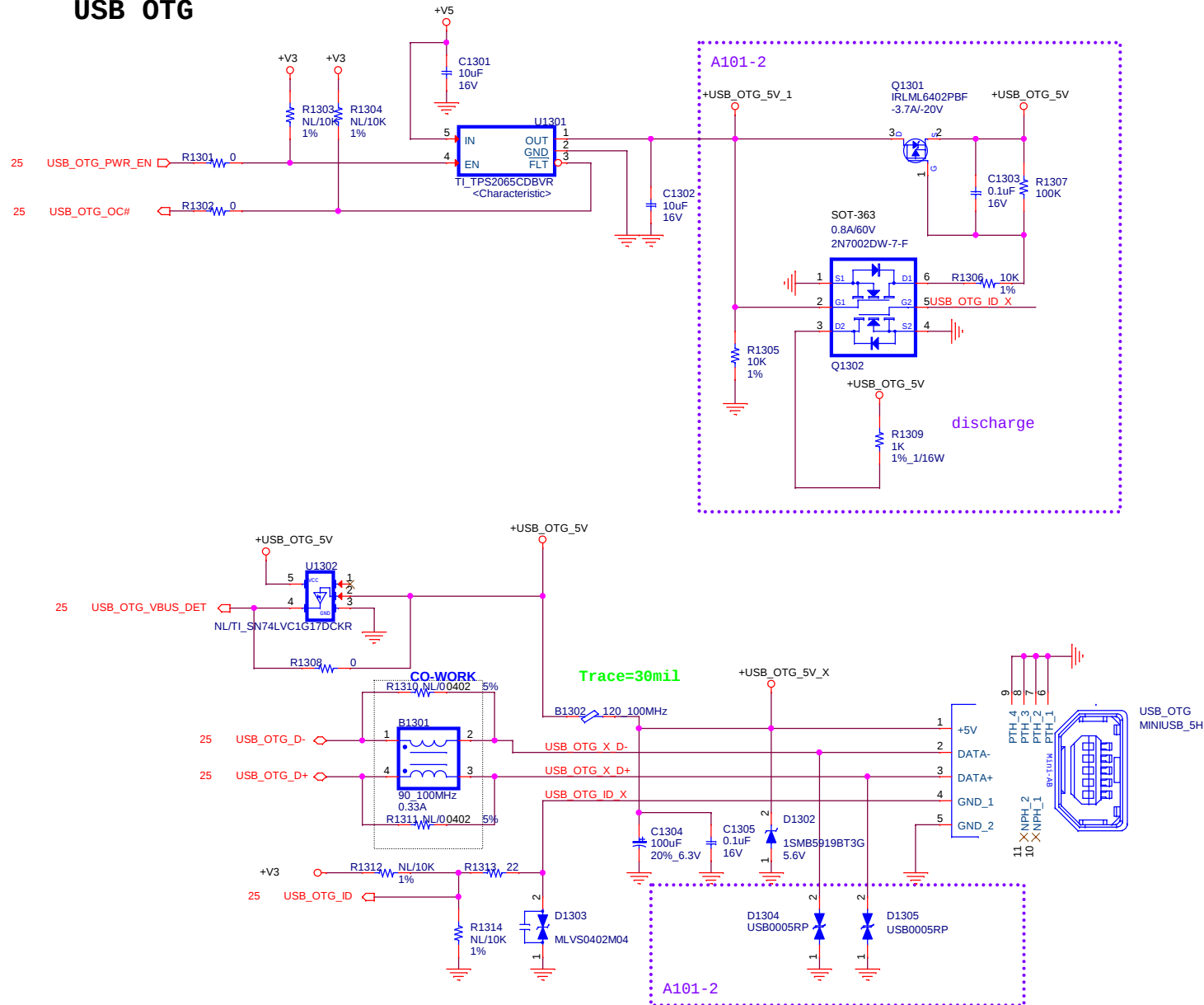


Close to HDMI connector

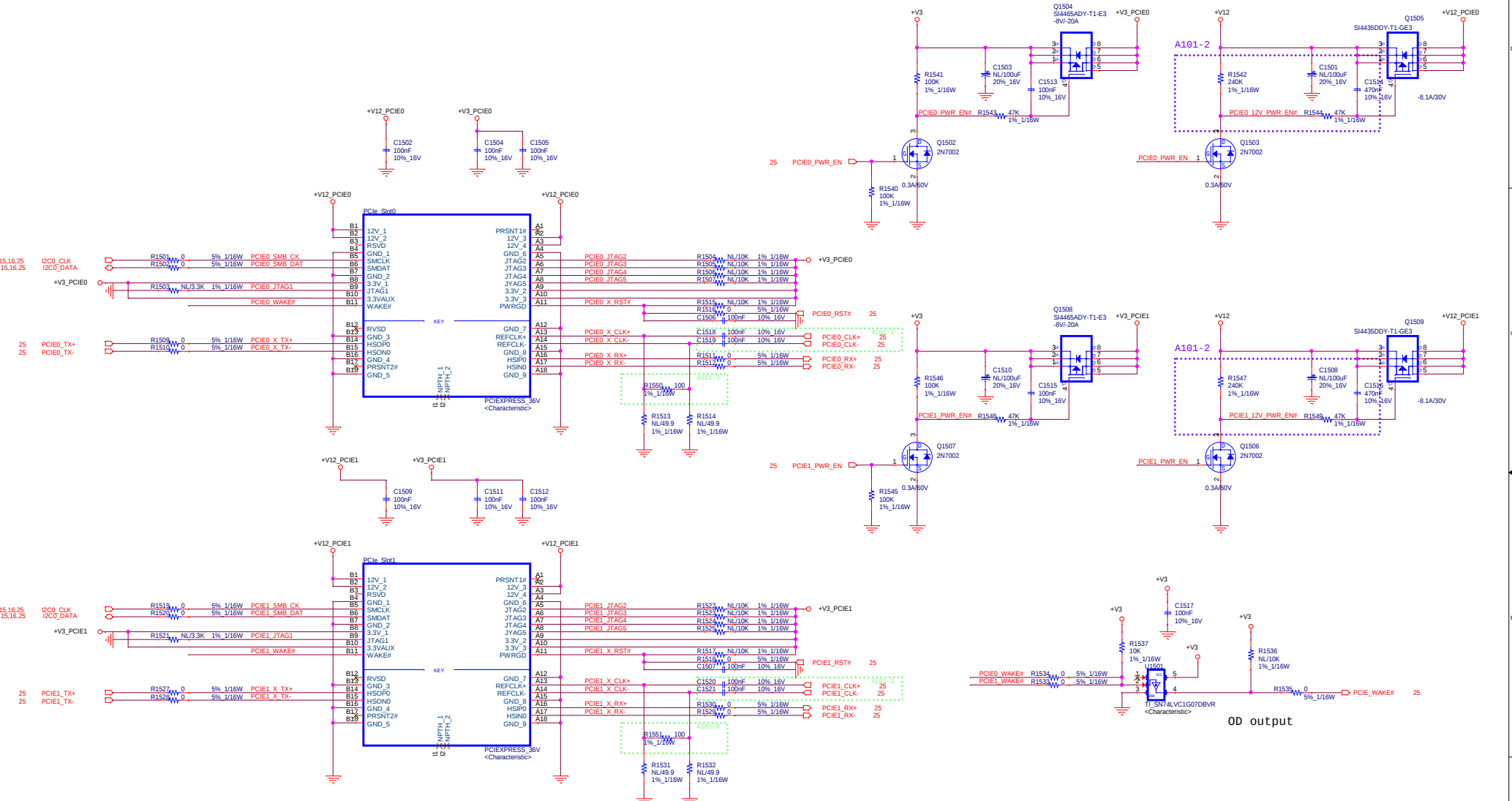


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Size	Document Number	ROM-DB3900	Rev
Date:	Friday, December 04, 2015	Sheet	12 of 26

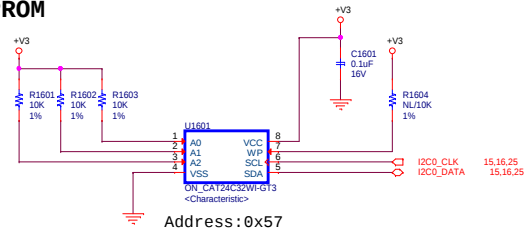
USB OTG



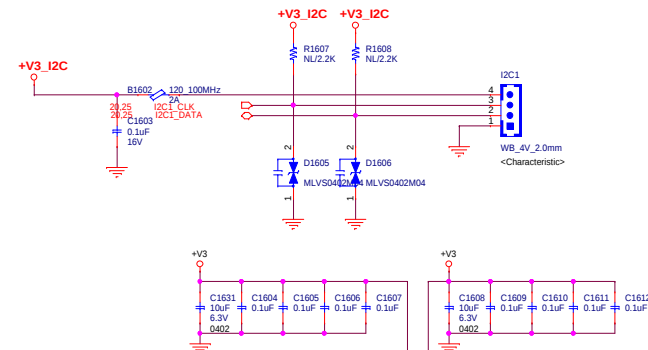
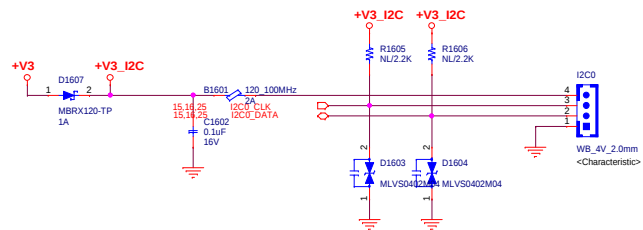
ADVANTECH			
Title USB OTG			
Size	Document Number	ROM-DB3900	
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EEPROM

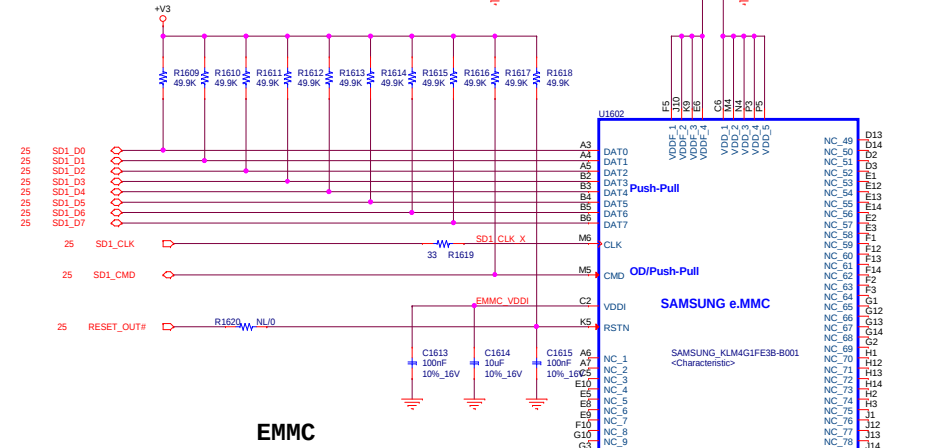
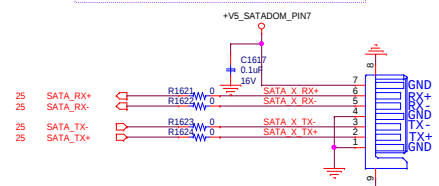
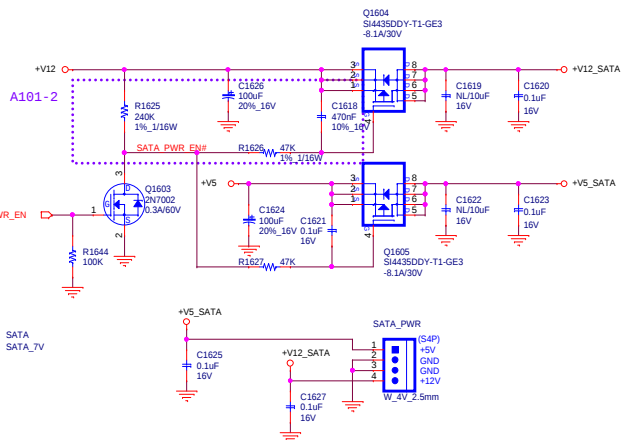
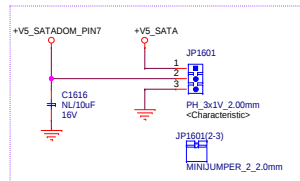


I2C Header

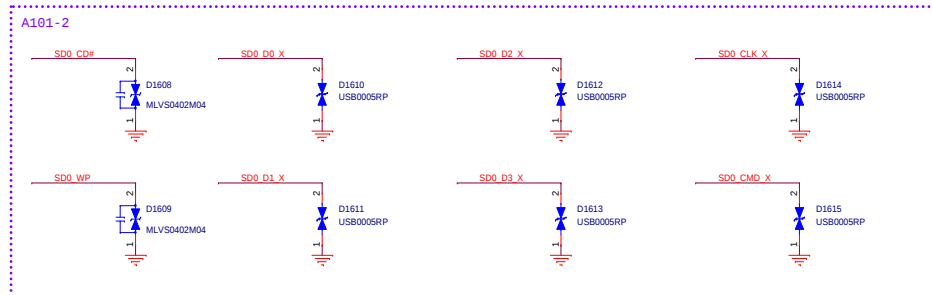
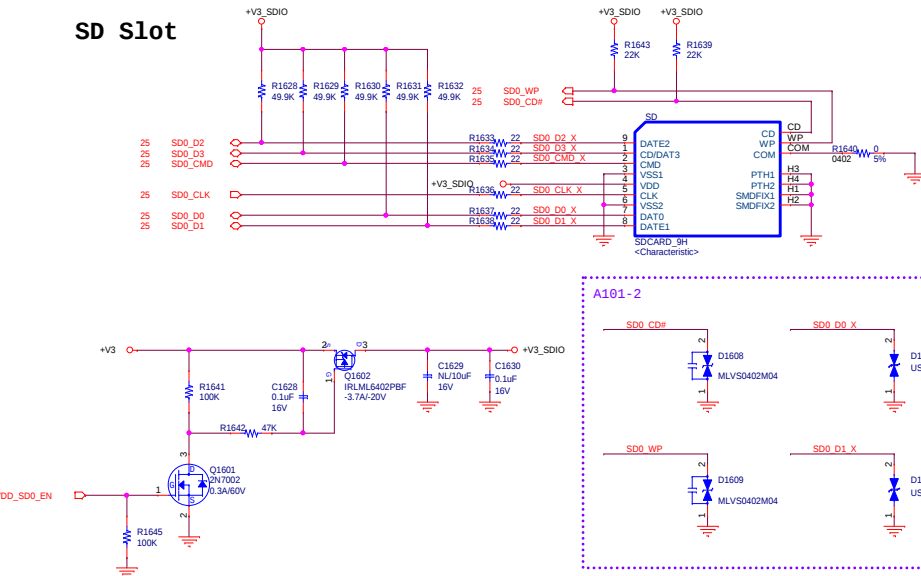


SATA DOM

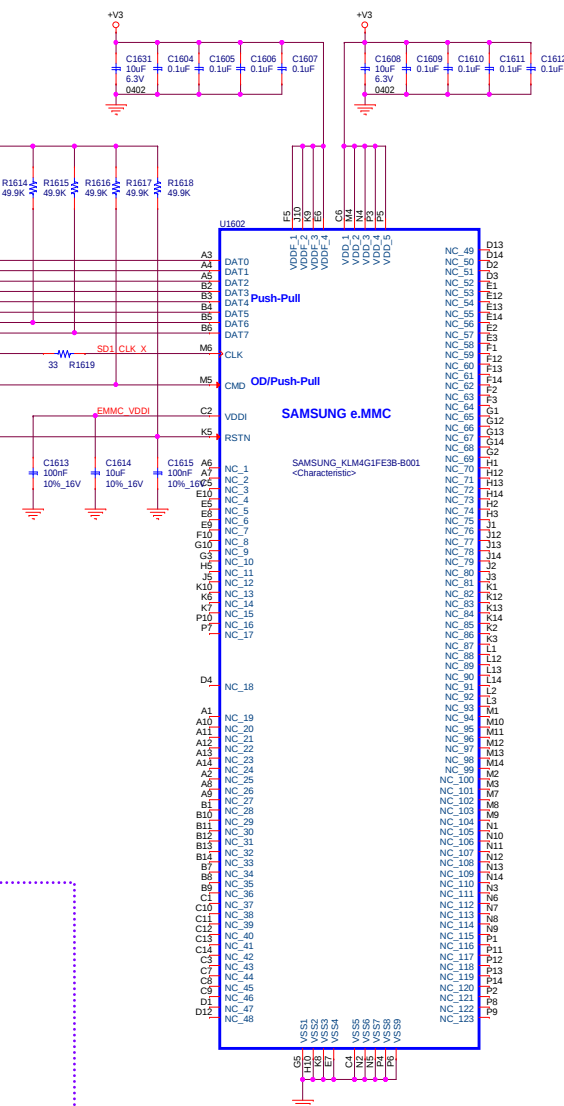
A101-2 change



SD Slot



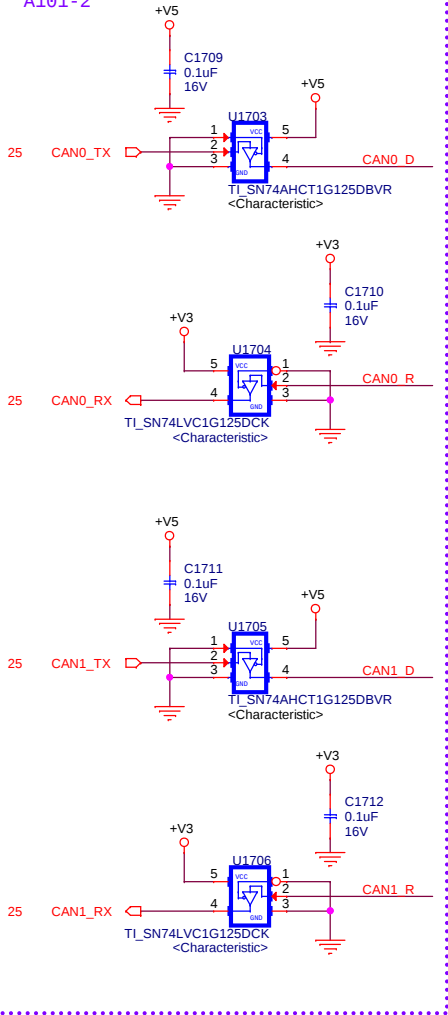
EMMC



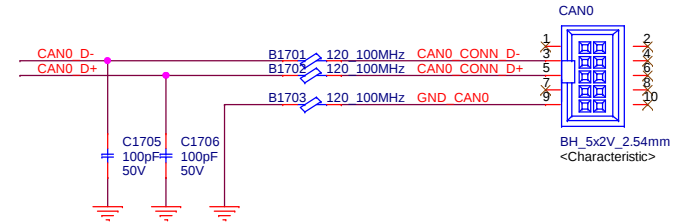
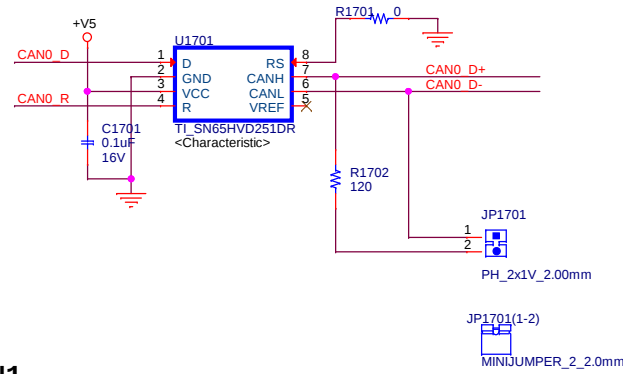
ADVANTECH
SATA, SDIO, EMMC, I2C EEPROM

Size: Document Number ROM-DB3900
Date: Friday, December 04, 2015 Sheet 16 of 26

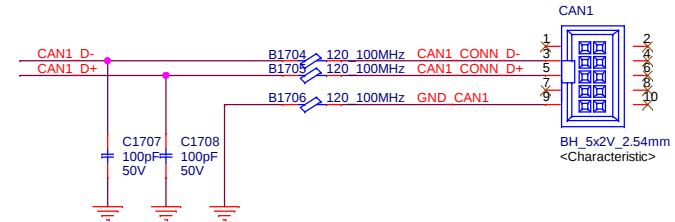
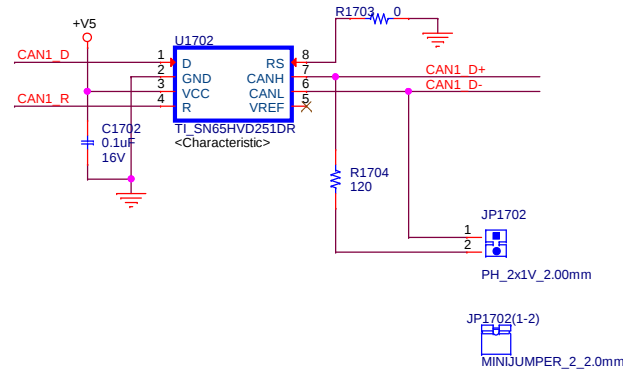
A101-2



CAN0

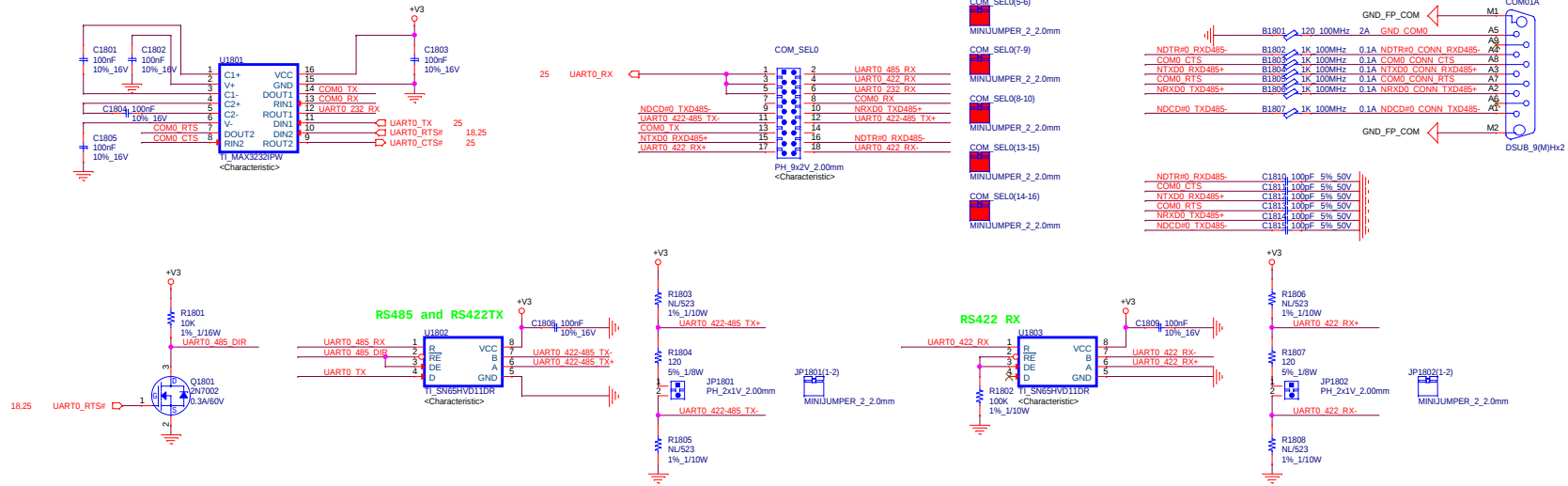


CAN1

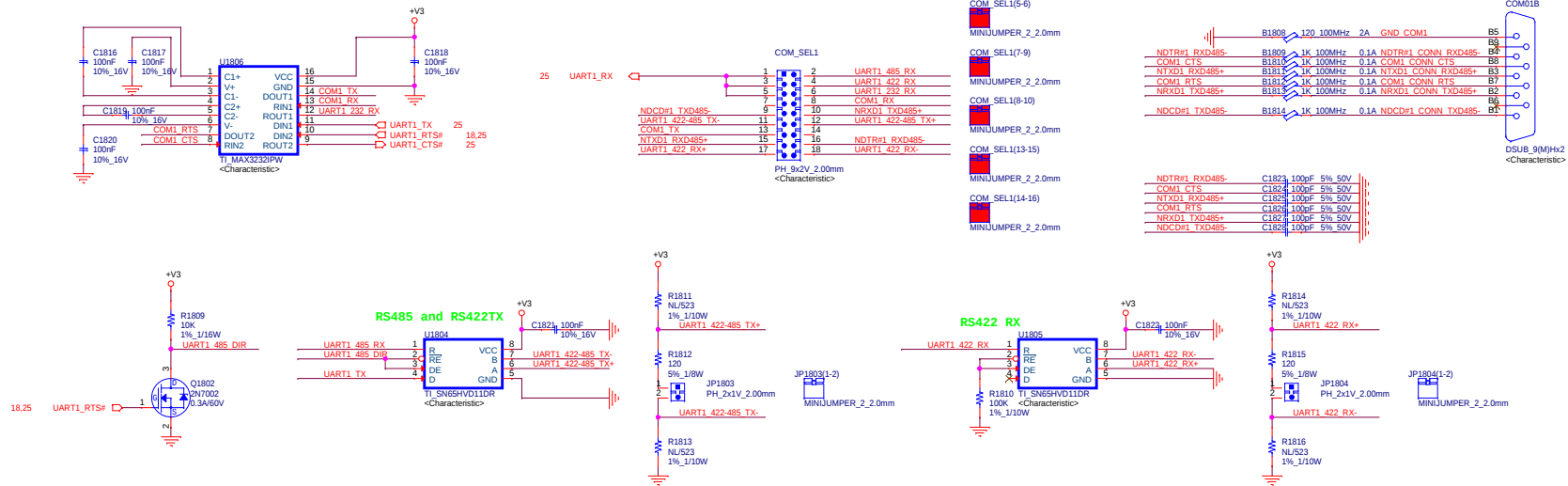


ADVANTECH			
Title			
CAN BUS			
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COM0:



COM1:



ADVANTECH

Title: UART0/1

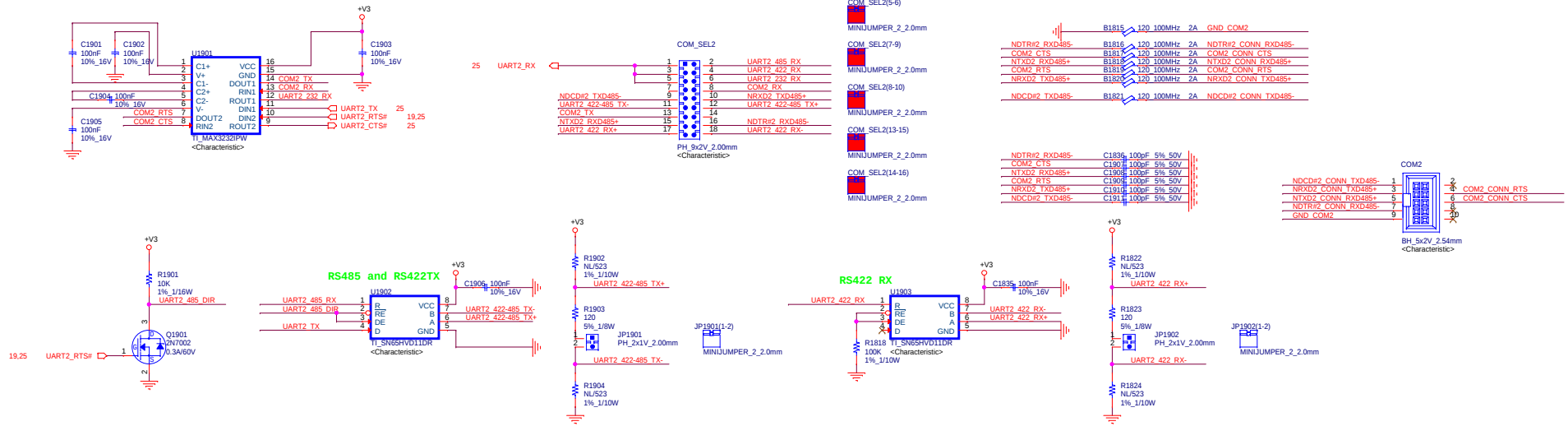
Size: Document Number: ROM-DB3900

Date: Friday, December 04, 2015

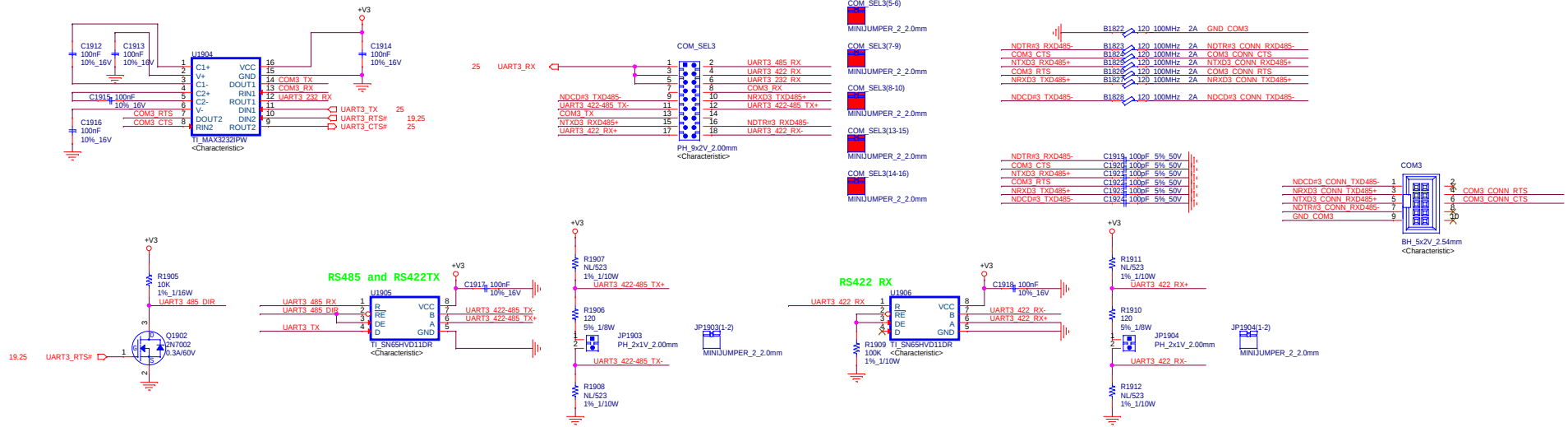
Sheet: 18 of 26

Rev: A101-3

COM2:



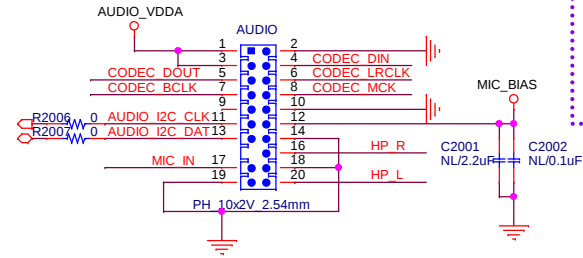
COM3:



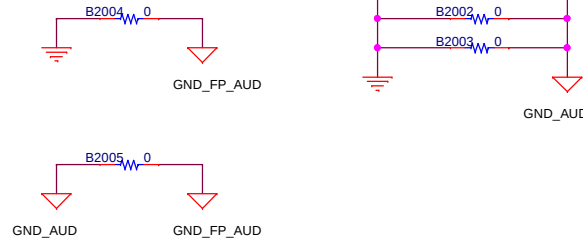
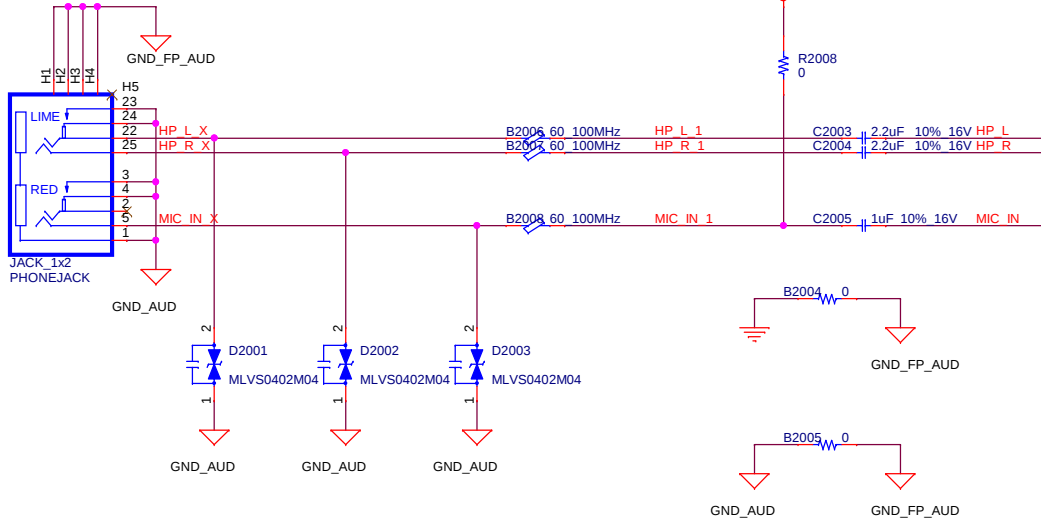
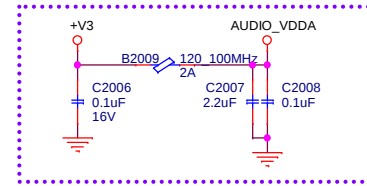
I2S connect to CODEC

25	I2S_DOUT	R2001	22	1%	1/10W	CODEC DOUT
25	I2S_DIN	R2002	22	1%	1/10W	CODEC DIN
25	I2S_BCLK	R2003	22	1%	1/10W	CODEC BCLK
25	I2S_LRCLK	R2004	22	1%	1/10W	CODEC LRCLK
25	I2S_MCLK	R2005	22	1%	1/10W	CODEC MCK

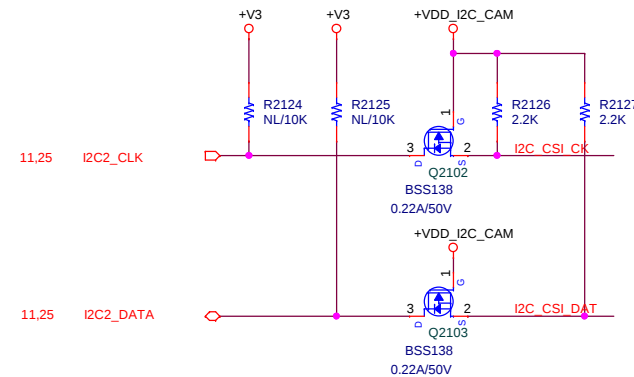
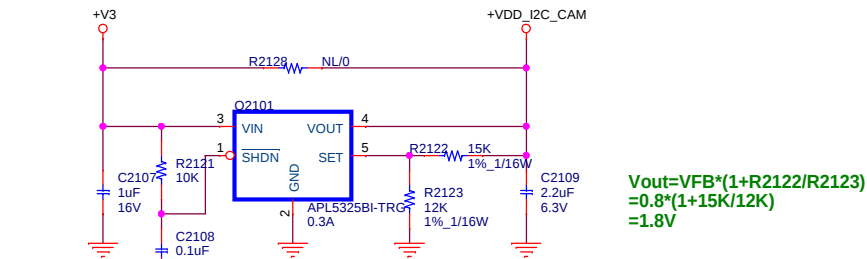
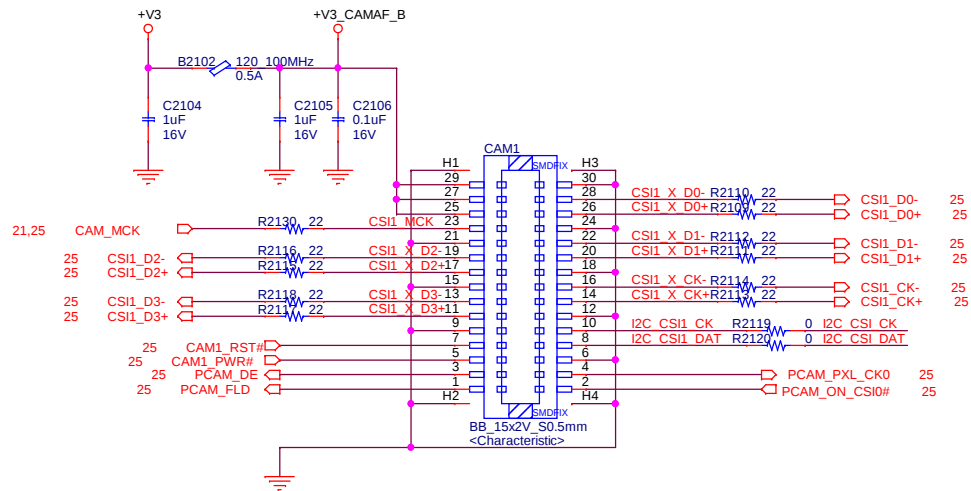
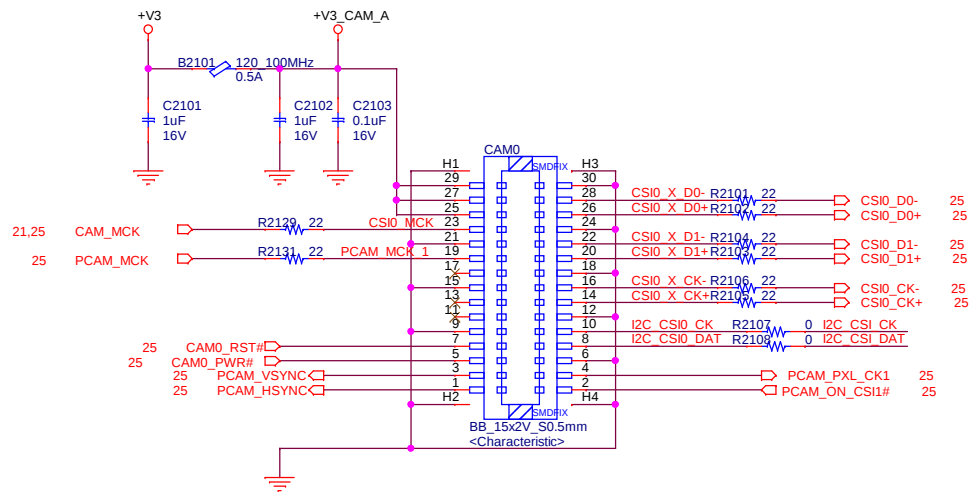
16,25 I2C1_CLK
16,25 I2C1_DATA



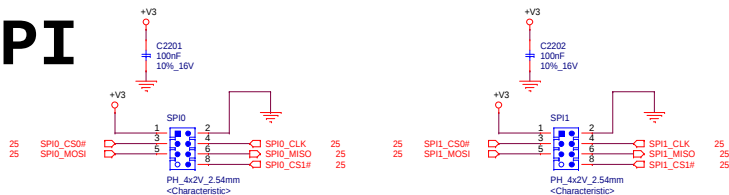
A101-2



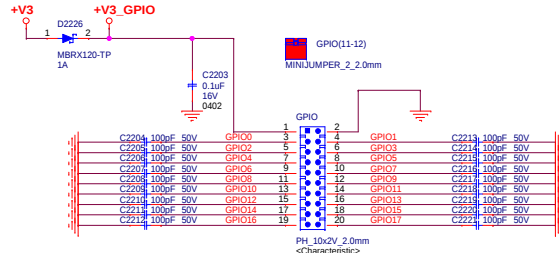
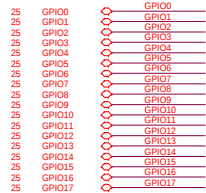
ADVANTECH			
Title	I2S		
Size	Document Number	ROM-DB3900	Rev
Date:	Friday, December 04, 2015	Sheet	20 of 26



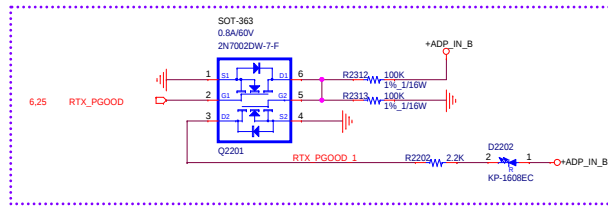
SPI



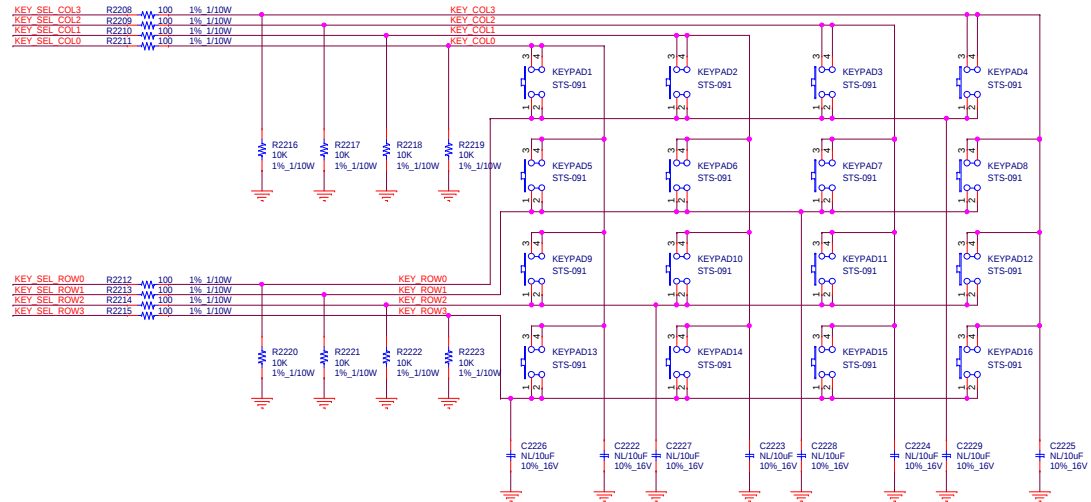
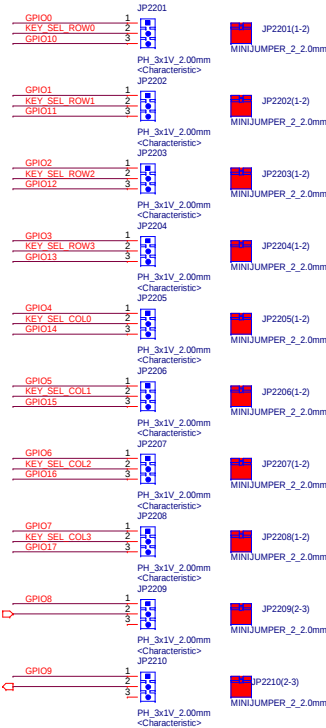
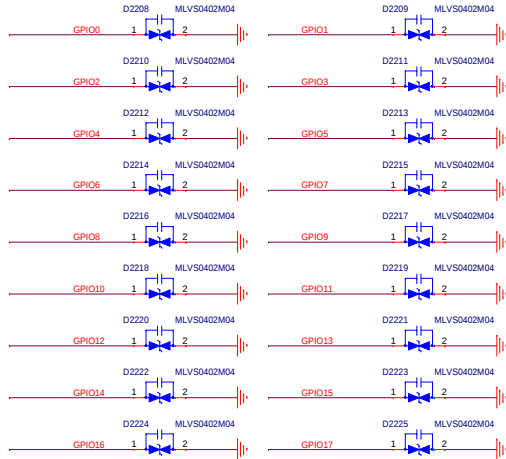
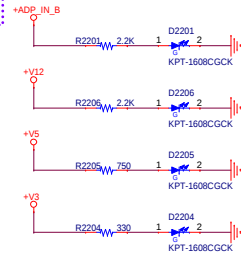
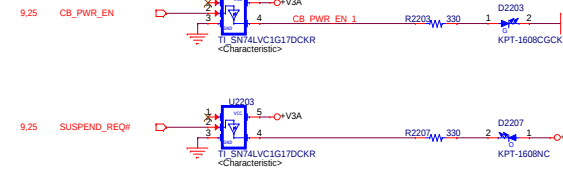
GPIO



A101-2



POWER LEDs



ADVANTECH
Title
SPI, LED, GPIO, Keypad

Size Document Number ROM-DB3900 Rev A101-3
Date Friday, December 04, 2015 Sheet 22 of 26

WAKE#

SW6
STS-091

C2307
10uF
10%_16V

SW2

1 8 BOOT_SEL0# X R2301 0.0402 5% BOOT_SEL0# 25

2 7 BOOT_SEL1# X R2302 0.0402 5% BOOT_SEL1# 25

3 6 BOOT_SEL2# X R2303 0.0402 5% BOOT_SEL2# 25

4 5 0V

EDG104S
<Characteristic>

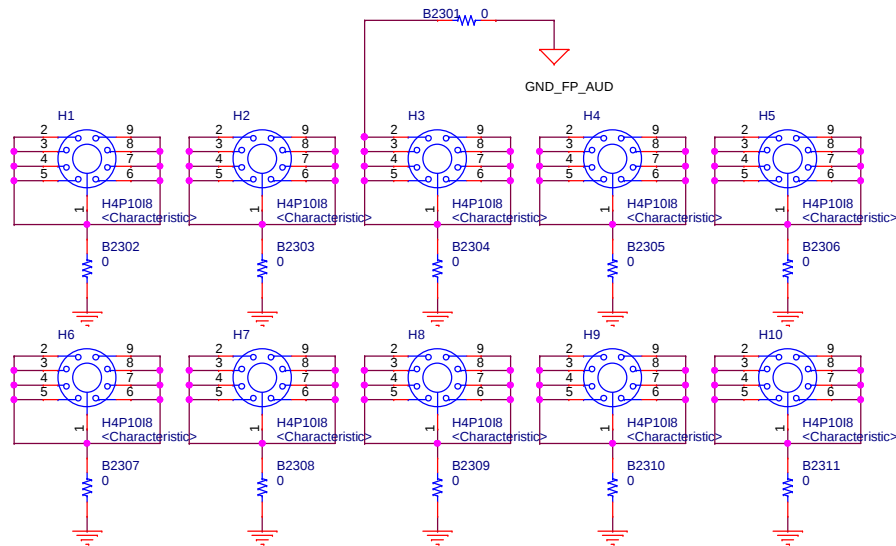
C2301 10uF 10%_16V

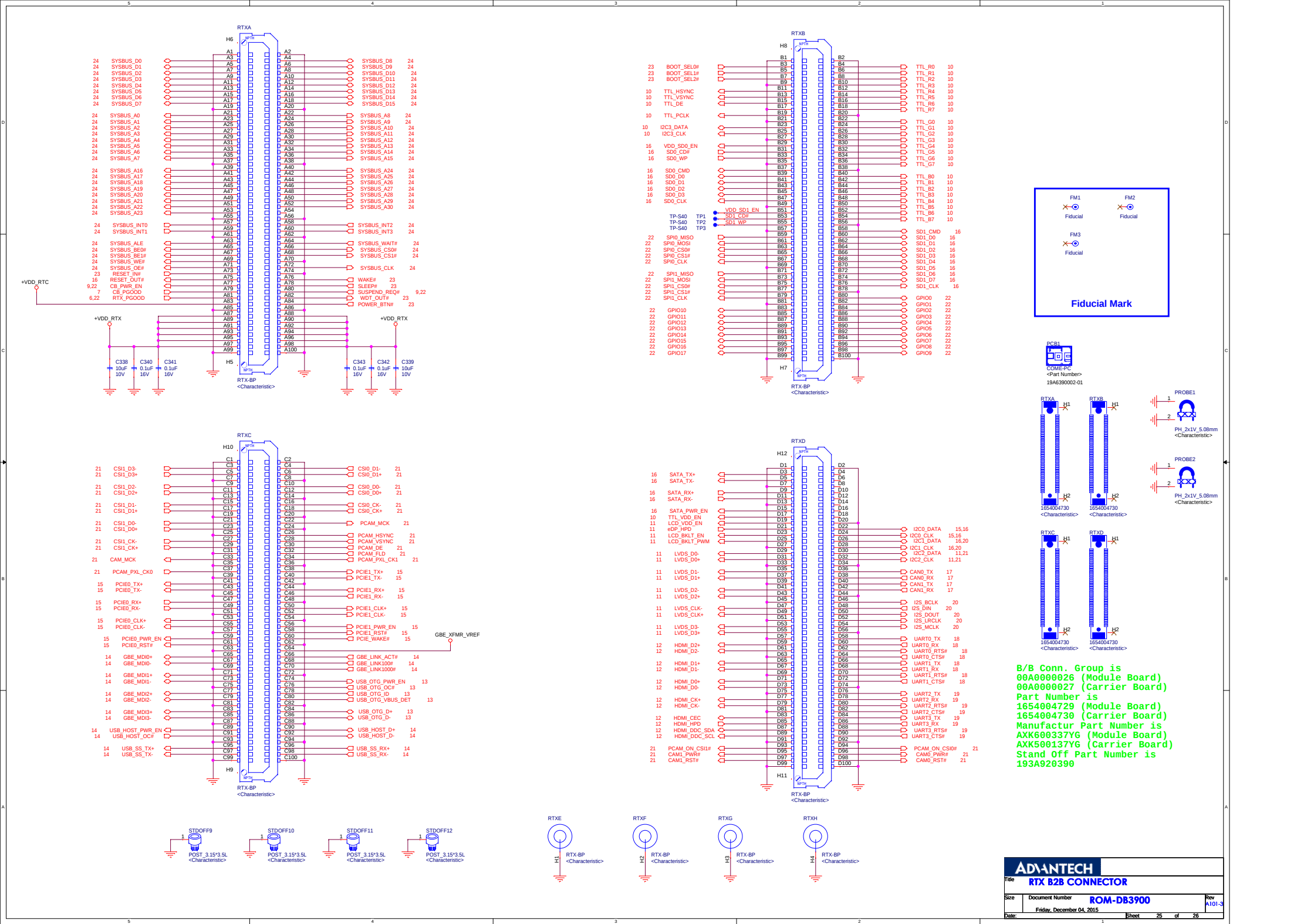
C2302 10uF 10%_16V

C2303 10uF 10%_16V

25 WDT_OUT#

JP2301
PH_2x1V_2.00mm

[illegible]



ROM-DB3900 A101-1 PCB:19A6390000-01, 96 BOM:9696M39000E Date: 2013/04/22

2013/04/22: Initial Release.

ROM-DB3900 A101-2 PCB:19A6390001-01, 96 BOM:9696M39000E Date: 2013/09/30

2013/09/23:

ROM-DB3900 A101-3 PCB:19A6390002-01, 96 BOM:9696M39000E Date: 2014/03/06

2014/02/14: Add reserve voltage protection. Change 12V buck controller. R610 replace with 25m ohm.
2014/02/14: U802, U902 replace by TI_SN74LVC1G07DBVR. U801, U901 (SC417) LDO are always ON. +V3 and +V5 control by EN/PSV pin.
2014/02/14: Add Q1003, Q1004 to prevent CH7055A VDDIO leakage current.
2014/02/14: All varistors for high speed signal replace by USB0005RP.
2014/02/14: Both PCIE clock add ac coupling capacitor. Add 100ohm terminal resistor between PCIE clock pair.
2014/02/14: Add R2401 for SOM-CMX53 UART testing.
2014/02/27: CAN0 & CAN1 change connector type. (1653205200)
2014/05/22: R610 replace by 20mohm to increase current limit protection (OCP) for RTX module.
2015/12/04: fix RTX_PGOOD offpage direction.